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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,365	09/30/2003	Chi-Yu Ho	BHT-3167-156	4348

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EXAMINER	
EISEN, ALEXANDER	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,365	HO ET AL.	
	Examiner	Art Unit	
	Alexander Eisen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it should be written in proper idiomatic English. Phrases like "A key inputting circuit is disclosed herein" should be avoided, because it is not an abstract, wherein a circuit is disclosed. Correction is required. See MPEP § 608.01(b).

Claim Objections

2. Claims 1-13 are objected to because of the following informalities:

- Claim 1 recites: "while pressing one of keys then an input reference voltage signal will have a predetermined drop". By looking at the figures and the specification, it is understood that the reference voltage is always the same, i.e. never changes (that is why it is called a reference voltage). What changes is a potential at a gathering terminal A (see paragraphs 17-18 of the specification). The appropriate choice of wording, such as, for example, - - ***when one of keys is pressed a potential at a gathering terminal will drop to a predetermined level defined by a specific number of resistors connected in series, causing a designated voltage signal to be output to an A/D converter*** - -, would overcome this objection.
- Note also that "resistances" are replaced by - - ***resistors*** - -, because "resistance" is a quantitative property of resistors, and as such is not a physical component, which could be connected in series. Claims 1, 4, 5, 8, 9 and 11 also use "resistances" instead of resistors and therefore all require an appropriate correction.

- Note also, that "output to a CPU" is replaced by - - ***output to an A/D converter*** - -, because that is where a designated voltage from a gathering terminal is output to. What is output to CPU is a digital representation of that voltage converted by A/D converter. Claims 5 and 9 have the same problem, "**a CPU**" should read in these claims - - **an A/D converter** - -.

  Appropriate correction is required.

While the examiner has pointed out on some deficiencies in claims, the Applicants are encouraged to review the specification, the abstract and claims in order to bring it to more viable form.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3, 5 and 7 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Symanow et al., US 5,999,104, hereinafter Symanow.

With respect to claims 1 and 5 Symanow discloses a key inputting circuit (see FIG. 5), wherein when one of keys 50-55 is pressed a potential at a gathering terminal (point of connection between a resistor 40 and a diode 59) will drop to a predetermined level defined by a specific number of resistors (41-47) connected in series, and a designated voltage signal will be output to an A/D converter 56. Symanow further discloses a load resistor 40 connected between the reference voltage source V_R and signal gathering terminal (see also col. 5, lines 1-21).

As pertaining to claims 3 and 7, Symanow discloses also A/D converter 56, which converts the designated voltage signal into digital value and transmits it to the CPU 60.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 6 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Symanow in view of Gulick, US 5,512,893.

With respect to claim to claims 2, 6 and 9 Symanow discloses a key inputting circuit (see FIG. 5), wherein when one of keys 50-55 is pressed a potential at a gathering terminal (point of connection between a resistor 40 and a diode 59) will drop to a predetermined level defined by a specific number of resistors (41-47) connected in series, and a designated voltage signal will be output to an A/D converter 56. Symanow further discloses a load resistor 40 connected between the reference voltage source V_R and signal gathering terminal (see also col. 5, lines 1-21).

As pertaining to claims 2, 6 and 9, Symanow does not discloses that the key inputting circuit or module further comprises a potential (voltage) comparator, which compares the reference voltage with the designated voltage and decides to enable the CPU.

In addition, as pertaining to claim 9, even though none of the cited references teaches two circuit boards and a CPU mounted on the first circuit board, it would have been obvious to one of ordinary skill in the art at the time when the invention was made that the components of the key inputting circuit can be placed on any number of circuit boards without detrimentally

effecting the performance, and would be simply dictated by a design choice and would not bring about any unexpected result.

Gulick teaches a key inputting circuit 251 (FIG. 1) for CPU having potential comparators 250 comparing the reference voltages with the designated voltages and sending out to CPU a wake-up signal (enabling CPU for processing the key entry; see FIG. 1; col. 6, lines 35-43; col. 6, line 62 – col. 7, line 67).

It would have been obvious to one of ordinary skill in the art at the time when the invention was made to improve the key inputting circuit of Symanow with the comparators taught by Gulick, because it would allow to implement shut-down/wake-up mode for the integrated circuits participating in key processing and therefore to save power (Id. Gulick; col. 6, lines 35-43).

As pertaining to claim 10, Symanow discloses also A/D converter 56, which converts the designated voltage signal into digital value and transmits it to the CPU 60.

As pertaining to claim 11, while Symanow discloses that the resistors are a resistive network (ladder), it does not specifically disclose that the resistors are selected from a group consisting of carbon film resistors, metal film resistors, or chip resistor. But to select the type of resistors for Symanow's network would be well within the skills of those of ordinary skill in the art at the time when the invention was made, and would not require undue experimentation or bring about any unexpected result.

As pertaining to claims 12-13, Gulick teaches that the key inputting circuit can be used in a communication device, namely portable phone (col. 22, lines 22-25).

7. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Symanow.

While Symanow discloses that the resistors are a resistive network (ladder), it does not specifically disclose that the resistors are selected from a group consisting of carbon film resistors, metal film resistors, or chip resistor. But to select the type of resistors for Symanow's network would be well within the skills of those of ordinary skill in the art at the time when the invention was made, and would not require undue experimentation or bring about any unexpected result.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hannaford, US 4,884,070, discloses a key inputting circuit similar to that of the invention.

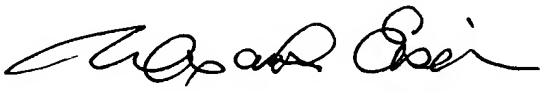
Nash et al., US 5,983,116, discloses a key input device similar to that of the invention and having at least two board circuits.

Nishimori et al., JP 63-206819, discloses two-boards device having resistive network, A/D converter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is (571) 272-7687. The examiner can normally be reached on M-F (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander Eisen
Primary Examiner
Art Unit 2629

24 March 2006